IN THE SPECIFICATION

Please replace paragraph 0002 with the following paragraph:

FIG. 1 shows a conventional transmission arrangement, in which digital data [[is]] **are** input to a digital-to-analog converter (DAC) 100. DAC 100 outputs an analog signal that changes value at discrete times determined by a clock signal CK as it clocks D-type flip-flops (not specifically shown) at the DAC's input. Being the result of discrete time clocking, the DAC's analog output signal has sharp vertical edges in the time domain.

Please replace paragraph 0003 with the following paragraph:

Undesirably, the presence of sharp edges in the DAC's analog output signal implies there is significant energy at harmonic frequencies (see FIG. 5A; which assumes a CK frequency of 1 GHz). To mask interfering emissions such as those at harmonic frequencies (as effectively mandated, for example, by the U.S. Federal Communications Commission, FCC), a low pass reconstruction filter 102 has conventionally been employed. Such a filter lowers **the** higher-frequency content of signals before sending them to a modulator 104 for generating a radio frequency (RF) modulated signal.

Please replace paragraph 0004 with the following paragraph:

The reconstruction filter is usually an analog filter that consumes a substantial amount of power, has large process/temperature/voltage variations (approximate ±30% for integrated passive R/C components), and is very difficult to design when the DAC input/output signal [[freq]] **frequency** is high. Furthermore, the closeness of the harmonic frequencies to the desired pass band, and the prevalence of higher energy content at lower harmonics (see FIG. 5A) have required filter 102 be complex.

Please replace paragraph 0021 with the following paragraph:

Briefly, the embodiment disclosed herein uses a current switch filtering technique to implement a discrete time ~~re-construction~~ **reconstruction** filter in a current steering digital-to-

analog converter (DAC). It takes advantage of current domain outputs of a current steering DAC, using multiple clock phases to "steer" (phase-adjust) and sum the currents in the resulting output. A result is discrete-time current-switched filter with a very accurate corner frequency.

Please replace paragraph 0024 with the following paragraph:

DFFs 301, 302 provide clocked digital output signals to respective current steering DACs 311, 312. Each of the two DACs may be, for example, half the size of a single DAC having the desired output differential current level. That is, differential currents from each DAC 311, 312 may be, for example, half of the desired *total* differential DAC current.

Please replace paragraph 0030 with the following paragraph:

FIG. 3B illustrates an approach to implementing DAC/filter 200 involving a general case of *N* current steering DACs. Digital data [[is]] **are** input to N sets of D-type flip-flops (DFFs), labeled 351, 352, 353...35N. DFFs 351, 352, 353...35N are clocked by respective clock signals $\varphi_1, \varphi_2, \varphi_3 \ldots \varphi_N$, that are provided by a suitable *N*-phase frequency source 340. In one embodiment illustrated in the timing diagram of FIG. 3C, the *N* phased clock signals φ are equally spaced apart in phase, and are clocked on the rising edge of the clock signals.

Please replace paragraph 0040 with the following paragraph:

As shown in FIG. 5B, waveform F results in a significant reduction in the odd-numbered images (1 GHz, 3 GHz, 5 GHz, and so forth). For example, the 1GHz image is reduced by a difference value Δ that is greater than 8 dB for the 1GHz-230MHz = 770MHz image that is closest to baseband. This degree of image rejection cannot readily be achieved by the conventional arrangement of FIG. 1, ~~at least~~ without a complex, sophisticated and costly filter 102.